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Description

VOLTAGE CONTROLLED OSCILLATOR (VCO) WITH AMPLITUDE CONTROL

Background of Invention

[0001] 1. Technical Field

[0002] The present invention relates to a structure and associated method to control an amplitude of oscillation in a voltage controlled oscillator.

[0003] 2. Related Art

[0004] Electrical circuits are typically required to control electrical signals to operate within specific operating boundaries. An inability to control an electrical signal to operate within specific operating boundaries may cause the electrical circuit to malfunction. Therefore there exists a need to control an electrical signal to operate within a specific operating boundary.

Summary of Invention

[0005] The present invention provides a voltage controlled oscil-

lator circuit, comprising:

[0006] a drive circuit;

[0007] an inductor/capacitor (LC) tank circuit, the LC tank circuit and the drive circuit collectively comprising a first oscillating node and a second oscillating node, the first oscillating node being adapted to have a first voltage, the second oscillating node being adapted to have a second voltage; and

[0008] a diode adapted to control an amplitude of the first voltage and an amplitude of the second voltage.

[0009] The present invention provides a method, comprising:

[0010] providing a drive circuit, an inductor/capacitance (LC) tank circuit, and a diode within a voltage controlled oscillator circuit, the drive circuit and LC tank circuit collectively comprising a first oscillating node and a second oscillating node; and

[0011] controlling by the diode, an amplitude of a first voltage at the first oscillating node and an amplitude of a second voltage at the second oscillating node.

[0012] The present invention advantageously provides a structure and associated method to control an electrical signal to operate within a specific operating boundary.

Brief Description of Drawings

[0013] FIG. 1 illustrates a block diagram view of a phase-locked loop (PLL) circuit comprising a voltage controlled oscillator (VCO) circuit, in accordance with embodiments of the present invention.

[0014] FIG. 2 illustrates an internal schematic of the VCO circuit of FIG. 1, in accordance with embodiments of the present invention.

[0015] FIG. 3 illustrates a modified internal schematic of the VCO circuit of FIG. 2, in accordance with embodiments of the present invention.

[0016] FIG. 4 illustrates a graph comparing a plot of an amplitude of oscillation with the amplitude control diode to a plot of an amplitude of oscillation without the amplitude control diode, in accordance with embodiments of the present invention.

Detailed Description

[0017] FIG. 1 illustrates a block diagram view of a phase-locked loop (PLL) circuit 2 comprising a phase frequency detector 4, a charge pump 7, a loop filter 9, and a voltage controlled oscillator (VCO) 11, in accordance with embodiments of the present invention. The phase frequency de-

tector 4 is electrically connected to the charge pump 7. The charge pump 7 is electrically connected to the loop filter 9. The loop filter 9 is electrically connected to the VCO 11. The VCO 11 is electrically connected to the phase frequency detector 4. The phase frequency detector 4 compares a phase and frequency of a reference signal 16 to a phase and frequency of a feedback signal 14 from the VCO 11. The phase frequency detector 4 generates an output comprising an increment (INC) pulse signal 19 and a decrement (DEC) pulse signal 20. The INC pulse signal 19 and the DEC pulse signal 20 represent the phase and frequency difference between the reference signal 16 and the feedback signal14. The feedback signal 14 is equivalent to the output signal 15. When a phase of the output signal15 is lagging a phase of the reference signal 16, a pulse width of the INC pulse signal 19 is set wider than a pulse width of the DEC pulse signal 20. When a phase of the output signal15 is leading of a phase of the reference signal 16, the pulse width of the DEC pulse signal 20 is set wider than the pulse width of the INC pulse signal 19. The INC pulse signal 19 and the DEC pulse signal 20 are transmitted to the charge pump 7. The INC pulse signal 19 and the DEC pulse signal 20 control the charge pump 7

to source or sink a current flow 33 to/from the loop filter 9. Based on an amount and the direction (i.e., source or sink) of the current flow, the loop filter 9 produces a control voltage 10. The control voltage 10 controls the VCO 11 to produce an output signal 15 that tracks the reference signal 16 (i.e., output signal 15 tracks a phase and frequency of the reference signal 16). The PLL circuit 2 is referred to as "locked" when the output signal 15 tracks the phase and frequency of the reference signal 16.

[0018] FIG. 2 illustrates an internal schematic of the voltage controlled oscillator (VCO) circuit 11 of FIG. 1, in accordance with embodiments of the present invention. Note that although the VCO circuit 11 of FIG. 1 and 2 is described with reference to the phase-locked loop (PLL) circuit 2 of FIG. 1, the VCO circuit 11 of FIG. 1 and 2 may be used in any electrical circuit requiring a VCO known to a person of ordinary skill in the art such as, inter alia, communications circuits, servo circuits, etc. The VCO circuit 11 comprises an inductor/capacitor (LC) tank circuit 39, a drive circuit 37, and a comparator 17. The LC tank circuit 39 comprises, an inductor 18, an inductor 21, a varactor 23, and a varactor 25. The inductor 18 is electrically connected between the varactor 23 and the inductor 21. The varactor

25 is electrically connected between the inductor 21 and the varactor 23. The drive circuit 37 comprises transistor 31 and a transistor 33. The transistor 31 and the transistor 33 may each be any transistor known to a person of ordinary skill in the art such as, inter alia, a field effect transistor (FET), an n-channel FET, a p-channel FET, a bipolar transistor, etc. The transistor 31 is electrically connected to the transistor 33 between the inductor 21 and the varactor 25 at an oscillation node 29. Additionally, the transistor 33 is electrically connected to the transistor 31 between the inductor 18 and the varactor 23 at an oscillation node 27. A voltage VDD provides a supply voltage for the VCO circuit 11. The current source 35 provides a current supply for the VCO circuit 11. During operation of the VCO circuit 11, the transistor 31, the varacter 23, and the inductor 18 collectively produce a first voltage at the oscillation node 27 and the transistor 33, the varacter 25, and the inductor 21 collectively produce a second voltage at the oscillation node 29. The first voltage and the second voltage are oscillating voltages that oscillate out of phase from each other. A frequency of the first voltage and the second voltage is controlled by the control voltage 10. The first voltage is applied to a first input

44 of the comparator 17. The second voltage is applied to a second input 47 of the comparator 17. The comparator 17 compares the first voltage to the second voltage and produces the output signal 15 that tracks the phase and frequency of the reference signal 16 of the phase lock loop circuit 2 of FIG. 1. A third voltage at node 41 comprises an average voltage of the first voltage at node 27 and the second voltage at node 29. The third voltage should comprise a mid supply voltage (i.e., VDD/2). An amplitude of oscillation (i.e., amplitude of the first voltage and the second voltage) is controlled by the transistors 31 and 33. When the first voltage and the second voltage comprise a high frequency (e.g., a frequency greater than 2500 Mhz), the amplitude of oscillation may increase to a voltage level that is higher than the supply voltage VDD or decrease to a level that is lower than ground (i.e., negative voltage) thereby exceeding the voltage bounds of the supply voltage VDD. The amplitude of oscillation may exceed the voltage bounds of the supply voltage VDD because of a faster switching time of the transistor 31 and the transistor 33 caused by the high frequency. If the amplitude of oscillation exceeds the voltage bounds of the supply voltage VDD the following conditions may occur:

[0019] 1. Assuming the transistor 31 and the transistor 33 are FETs, an oxide breakdown within the transistor 31 and the transistor 33 may occur thereby causing the transistor 31 and/or the transistor 33 to become damaged.

[0020] 2. Assuming the transistor 31 and the transistor 33 are FETs, a forward bias of pn junctions within the transistor 31 and the transistor 33 may occur causing a CMOS latchup.

[0021] 3. A changing amplitude of oscillation with a changing oscillation frequency may reduce a range of frequencies that the VCO 11 may attain.

[0022] The amplitude of oscillation should be limited to between the supply voltage VDD and ground to prevent the aforementioned conditions. A method to control an amplitude of oscillation is described in the description of FIG. 3, supra.

[0023] FIG. 3 illustrates a modified internal schematic of the voltage controlled oscillator (VCO) circuit 11 of FIG. 2 represented by the VCO 11A, in accordance with embodiments of the present invention. Note that although the VCO circuit 11A of FIG. 3 is described with reference to the phase-locked loop (PLL) circuit 2 of FIG. 1, the VCO circuit 11A of FIG. 3 may be used in any electrical circuit requir-

ing a VCO known to a person of ordinary skill in the art such as, inter alia, communications circuits, servo circuits, etc. In contrast with the VCO circuit 11 of FIG. 2, the VCO circuit 11A of FIG. 3 comprises a diode 44. The diode 44 in FIG 3 comprises a FET (n-channel (NFET), p- channel FET (PFET), etc) with a gate electrically shorted to a drain such that the FET functions as a diode. Note that the diode 44 may comprise any diode known to a person of ordinary skill in the art. Additionally, the diode 44 may comprise a bipolar transistor with a base shorted to a collector such that the bipolar transistor functions as a diode. The diode 44 is electrically connected in with the LC tank circuit 39 and the drive circuit 37. As the amplitude of oscillation of the first voltage at the first node 27 and the second voltage at the second node 29 increases or decreases, the third voltage at node 41 also increases or decreases accordingly. The diode 44 limits an amplitude of the first voltage and the second voltage by limiting an amplitude of the third voltage at node 41 (the third voltage is an average of the first voltage and the second voltage). The diode 44 limits an amplitude of the third voltage by shunting to ground any extra current away from the transistor 31 and the transistor 33. As the am-

plitude of oscillation increases, the third voltage on node 41 increases and the diode 44 conducts more current thereby reducing the amplitude of oscillation. Likewise, as the amplitude of oscillation decreases, the third voltage on node 41 decreases and the diode 44 conducts less current thereby increasing the amplitude of oscillation. During a temperature change to any of the circuitry within the VCO 11A (e.g, drive circuit 37, tank circuit 39, diode 44, etc.), the diode 44 maintains an about constant amplitude of oscillation. An about constant amplitude of oscillation is defined herein including in the claims as an amplitude that does not vary over time by more than 300 millivolts. Additionally, the diode 44 maintains an about constant amplitude of oscillation during a change of oscillation frequency or when the oscillation frequency comprises a high frequency (e.g., a frequency greater than 2500 Mhz). The nearly constant amplitude of oscillation is shown by the graph in FIG. 4 as described, supra.

[0024] FIG. 4 illustrates a graph comparing a plot 50 of an amplitude of oscillation with the diode 44 to a plot 52 of an amplitude of oscillation without the diode 44, in accordance with embodiments of the present invention. The X-axis represents time in arbitrary units. The Y-axis repre-

sents voltage in millivolts. The plot 55 represents a supply voltage VDD of 1200 millivolts. It can be seen from the plot 52 that the amplitude of oscillation rises above the supply voltage VDD 55 and below ground (less than 0 volts). Additionally, the plot 52 does not maintain an almost constant amplitude of oscillation (i.e., amplitude varies by more than 300 millivolts over time). It can be seen from the plot 50 that the amplitude of oscillation with the diode 44 stays within the voltage bounds of the supply voltage VDD (i.e., between VDD and ground). Additionally, the plot 50 does maintain an about constant amplitude of oscillation (i.e., amplitude does not vary by more than 300 millivolts over time).

[0025] While embodiments of the present invention have been described herein for purposes of illustration, many modifications and changes will become apparent to those skilled in the art. Accordingly, the appended claims are intended to encompass all such modifications and changes as fall within the true spirit and scope of this invention.